CLAIMS

What is claimed is:

1. An ESD (Electro Static Discharge) protection circuit, comprising:

a resistor device, wherein one end of the resistor devices is connected to a power supply;

a capacitor device, which is connected in series between the resistor device and ground; and

a PMOS device, which comprises a gate electrode, a first electrode, a second electrode and a bulk electrode, wherein the gate electrode is connected between the resistor device and the capacitor device, the bulk electrode is interconnected to the first electrode, and the first electrode is connected to the power supply.

2. The ESD protection circuit as claimed in claim 1, wherein the resistor device and the capacitor device form a RC circuit, and the rise time of the RC circuit is substantially between 0.1μs and 10μs.

3. An ESD protection circuit for multiple power supplies, comprising:

at least two ESD protection circuits, wherein each of the ESD protection circuits comprises:

a resistor device, wherein one end of the resistor device is connected to a power supply,

a capacitor device, which is connected in series between the resistor

device and ground,

a PMOS device, which comprises a gate electrode, a first electrode, a second electrode and a bulk electrode, wherein the gate electrode is connected between the resistor device and the capacitor device, the bulk electrode is interconnected to the first electrode, and the first electrode is connected to the power supply, and

each of the ESD protection circuits is connected to one of the multiple power supplies; and

a common ESD bus, wherein the second electrodes are connected to the common ESD bus.

4. The ESD protection circuit for multiple power supplies as claimed in claim 3, wherein the resistor device and the capacitor device in each of the ESD protection circuits form a RC circuit, and the rise time of the RC circuit is substantially between 0.1μs and 10μs.

5. The ESD protection circuit for multiple power supplies as claimed in claim 3, wherein the voltages of the multiple power supplies are equal to each other.

6. The ESD protection circuit for multiple power supplies as claimed in claim 3, wherein the voltages of the multiple power supplies are not equal.

7. The ESD protection circuit for multiple power supplies as claimed in claim 3, wherein there is no current flowing through the common ESD bus when the circuit is normal operated.